PCB Design Guideline Topics

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Introduction

We use **"pattern classes"** and **"drill classes"** as convenient shorthand to measure the manufacturability of the PCB.

This will define whether your board can be Pooled or not, it also has an impact on the pricing.

Pattern Classes

The pattern class covers the minimum sizes for copper track (conductor) and gap (isolation) for Outer and Inner layers:

Outer layer

- ***OTT*** *= Track to Track*
- ***OTP*** *= Track to Pad*
- ***OPP*** *= Pad to Pad*
- ***OTW*** *= Track Width*

Inner layer

- ***ITT*** *= Track to Track*
- ***ITP*** *= Track to Pad*
- ***IPP*** *= Pad to Pad*
- ***ITW*** *= Track Width*

The minimum copper rings on outer and inner layers

- ***OAR*** *= Outer Annular Ring*
- ***IAR*** *= Inner Annular Ring*

The minimum IPI (Inner layer Pad Isolation)

- **IPI** is the clearance between the edge of any unconnected hole (plated or non-plated) and the nearest copper (plane, track, pad).
- This is measured from the production tool size (actual drill or rout bit diameter).
- The minimum **IPI** value is always **IAR** + 0.075mm, with a minimum of 0.200mm.

- Thicker copper needs a wider isolation for reliable etching.
- The highest pattern class possible depends on the copper thicknesses.
- Not all copper thicknesses are available in all services.

For more information please see our current Classification table on below.

DRILL CLASSES

The Drill class is based on the smallest production drill size (**TOOLSIZE)** used to manufacture your board,.

This is not to be confused with the finished size hole size (**ENDSIZE**) that you have defined in your design/CAD system.

For more information on holes sizes and how to calculate the **TOOLSIZE** vs the **ENDSIZE** please refer to our PCB Design Guidelines – Drilled Holes page.

IMPORTANT

- The smallest of these values determines the pattern class.
- The Classification table shows the lower limit values of any given class.
- The Annular Ring values OAR and IAR in the Classification table are for plated holes (PTH).
- For connected non-plated (NPTH) holes we recommend a minimum annular ring of 0.30mm (300µm or 12mil).
    - As NPTH holes have no plated barrel, a smaller annular ring may lift during soldering or break away even during normal operating conditions.

For more information please see our current Classification table on below.

Recommendations

- Do not design your board up to the limits of any given classification.
- Always allow for a small margin above the classification limits, this will allow for any rounding errors etc.
- for more information please see our PCB Design Guidelines – Input Data Requirements page.

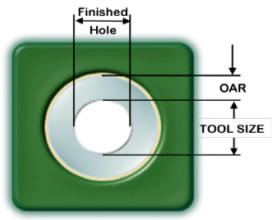
Classification Table

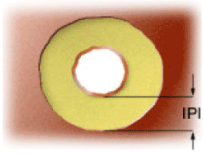
Eurocircuits - PCB Design Classification Overview

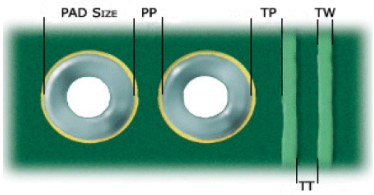
Pattern Class	class 3		class 4		class 5		class 6		class 7		class 8		class 9		class 10	
Service	All Services								S + DZ + RF + SF		S + DZ + RF				-	
	mm	mil	mm	mil	mm	mil	mm	mil	mm	mil	mm	mil	mm	mil	mm	mil
OTW	0.250	10	0.200	8	0.175	7	0.150	6	0.125	5	0.100	4	0.090	3.5	<0.090	<3.5
OTT-OTP-OPP	0.250	10	0.200	8	0.175	7	0.150	6	0.125	5	0.100	4	0.090	3.5	<0.090	<3.5
OAR	0.200	8	0.150	6	0.150	6	0.125	5	0.125	5	0.100	4	0.100	4	<0.100	<4
ITW	0.250	10	0.200	8	0.175	7	0.150	6	0.125	5	0.100	4	0.090	3.5	<0.090	<3.5
ITT-ITP-IPP	0.250	10	0.200	8	0.175	7	0.150	6	0.125	5	0.100	4	0.090	3.5	<0.090	<3.5
IAR	0.200	8	0.150	6	0.150	6	0.125	5	0.125	5	0.125	5	0.100	4	<0.100	<4
IPI	0.275	11	0.225	9	0.225	9	0.200	8	0.200	8	0.200	8	0.200	8	<0.200	<8

The smallest value (**OTW, OTT-OTP-OPP, OAR, ITW, ITT-ITP-IPP, IAR, IPI**) determines the **Pattern Class** of the board

Base Cu		min Pattern Values			
Base Cu OL		OTT-OTP-OPP		OTW	
		mm	mil	mm	mil
12µm	⅓oz	0.090	3.5	0.090	3.5
18µm	½oz	0.100	4	0.090	3.5
35µm	1oz	0.125	5	0.125	5
70µm	2oz	0.200	8	0.200	8
105µm	3oz	0.250	10	0.250	10
Base Cu IL		ITT-ITP-IPP		ITW	
12µm	⅓oz	0.090	3.5	0.090	3.5
18µm	½oz	0.100	4	0.090	3.5
35µm	1oz	0.125	5	0.125	5
70µm	2oz	0.200	8	0.200	8
105µm	3oz	0.250	10	0.250	10







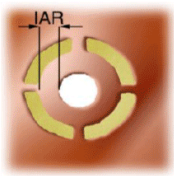
Preceding letters **O** and **I** stand for Outer- and Inner layer
Example: **OTW** = **O**uter layer **T**rack **W**idth

OAR : smallest **OAR** (Outer layer Annular Ring = 1/2 (Outer layer pad diameter - **TOOLSIZE**))
IAR : smallest **IAR** (Inner layer Annular Ring = 1/2 (Inner layer pad diameter - **TOOLSIZE**))
IPI (Inner layer **P**ad **I**nsulation) : Clearance between edge **TOOLSIZE** of any unconnected hole(PTH/NPTH) and any nearest copper

Smallest **TOOLSIZE** = Finished Hole Size + 0.10mm/4mil for **P**lated **T**hrough **H**oles
+ 0.00mm/0mil for **N**on **P**lated **T**hrough **H**oles

Drill Class	class A		class B		class C		class D		class E		class F	
Service	ALL Services		P + S + DZ + RF + SF + B				S +DZ + RF + SF				-	
	mm	Inch	mm	Inch	mm	Inch	mm	Inch	mm	Inch	mm	Inch
PTH	0.50	0.020	0.35	0.014	0.25	0.010	0.15	0.006	0.10	0.004	<0.10	<0.004
NPTH	0.60	0.024	0.45	0.018	0.35	0.014	0.25	0.010	0.20	0.008	<0.20	<0.008
min TOOLSIZE	0.60	0.024	0.45	0.018	0.35	0.014	0.25	0.010	0.20	0.008	<0.20	<0.008

NOTE: The smallest value (**TOOLSIZE**) determines the **Drill Class** of the PCB



Max. PCB Thickness to Drill Class	mm	Inch	mm	Inch	mm	Inch	mm	Inch	mm	Inch	
	3.20	0.125	3.20	0.125	2.40	0.093	2.00	0.079	1.60	0.062	Aspect Ratio is 1:8 (Based on the TOOLSIZE)

Note A: VIA holes are Plated Through Holes, default defined as <=0.45mm (18mil) for all services or <= as defined by the customer in the order details.
VIA holes have a maximum negative tolerance of 0.30mm (12mil)

Note B: This classification table can only be put into praxis on PCB designs that have a **Plating Index of 0.40 or higher.** This is calculated in the PCB Visualizer analysis and displayed in the PCB Visualizer order details.

Services Index : **P** = PCB proto **S** = STANDARD pool **DZ** = DEFINED IMPEDANCE **RF** = RF pool **SF** = SEMI-FLEX pool **I** = IMS pool **B** = BINDI pool

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Modified – Classification Table – Changed minimum IAR value for Pattern Class 9 & 10

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